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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3528US (97-1099)
First Inventor or Application Identifier	Alan R. Reinberg
Title	ELECTRICAL AND THERMAL CONTACT FOR USE IN SEMICONDUCTOR DEVICES
Express Mail Label No.	EL206385914US

APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages 26
(preferred arrangement set forth below)
-Descriptive title of the invention
-Cross References to related Applications
-Statement Regarding Fed Sponsored R&D
-Reference to Microfiche Appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings *(if filed)*
-Detailed Description
-Claim(s)
-Abstract of the Disclosure

3. ☒ Drawing(s) *(35 USC 113)* Total Sheets 5

4. Oath or Declaration Total Pages 1
a. ☒ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63(d))
(For continuation/divisional with Box 17 completed)
(Note Box 5 below)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☒ 37CFR 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement (IDS/PTO-1449) ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(If foreign priority is claimed)
16. ☐ Other: . . . . . .
. . . . . .
*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior Application No. _
Prior application information: Examiner _____ Group/Art Unit: ___

18. CORRESPONDENCE ADDRESS

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PTO/SB/17 (1/98)
Approved for use through 9/30/2000 OMB 0651-0032
Patent and Trademark Office: U S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT ($) 2152.00

Complete if Known	
Application Number	
Filing Date	November 9, 1998
First Named Inventor	Alan R. Reinberg
Examiner Name	
Group / Art Unit	
Attorney Docket No.	3528US(97-1099)

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-1469
Deposit Account Name: Trask, Britt & Rossa

[X] Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17
[ ] Charge the Issue Fee Set in 37 CFR 1 18 at the Mailing of the Notice of Allowance

2. [X] **Payment Enclosed:**
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims	67 -20** =	47	X 22	= 1034
Independent Claims	7 - 3** =	4	X 82	= 328
Multiple Dependent				=

***or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 1362.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	Brick G. Power			Reg. Number	38,581
Signature	Brick Power	Date	11/9/98	Deposit Account User ID	20-1469

PATENT
Attorney Docket 3528US (97-1099)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL206385914US

Date of Deposit with USPS: November 9, 1998

Person making Deposit: Jared Turner

APPLICATION FOR LETTERS PATENT

for

ELECTRICAL AND THERMAL CONTACT FOR USE IN SEMICONDUCTOR DEVICES

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ELECTRICAL AND THERMAL CONTACT FOR USE IN SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an electrical and thermal contact for use in semiconductor devices. Particularly, the present invention relates to an electrical and thermal contact which reduces the amount of energy input that is required in order to switch a semiconductor device structure that is contacted thereto between two or more states. More specifically, the electrical and thermal contact of the present invention includes thin conductive layers which envelop an insulator component. The electrical and thermal contact is particularly useful for switching contacted structures that include a phase change component between two or more states of electrical conductivity.

Background of Related Art

Electrically erasable programmable memory devices (EEPROMS) typically include several memory elements that may be switched between a first logic state and a second logic state. A first logic state may be an inactive state, or an "off" state, wherein electrical impulses do not travel across the memory element. Memory elements may be said to be in a second logic state, such as an "activated" state or an "on" state, when low voltage electrical impulses (i.e., of the operational voltage of the EEPROM) will readily travel thereacross.

Memory elements may comprise fuse elements or antifuse elements. Fuse elements are programmed by "blowing" (i.e., breaking the electrical connection across) the fuse thereof, which switches the fuse elements from an active state to an inactive state. Conversely, antifuse elements are programmed by forming a low resistance electrical path across (i.e., activating) the antifuses thereof. The programming of both fuse and antifuse elements requires the application of a sufficient current and voltage to such memory elements. Nevertheless, the application of too great a current to memory elements, such as fuse and antifuse elements, increases the potential that various other components of the EEPROM of which they are a part, including without limitation the

gate oxide layer, transistors, and other structures on the surface thereof, may be damaged.

FIG. 1 is a schematic representation of an exemplary conventional antifuse element 1, which includes a metal contact 2, first and second electrodes 4 and 8, respectively, and a dielectric layer 6, which electrically insulates the first electrode 4 from the second electrode 8. Metal contact 2 is typically a large element relative to the remainder of antifuse element. As a current is applied to metal contact 2, the resistance that is generated thereby and by at least one of the electrodes 4, 8 that are in contact therewith locally heats dielectric layer 6, destroying at least a portion of the same and facilitating the formation of an electrically conductive pathway between first electrode 4 and second electrode 8. Thus, an electrical contact is established between first and second electrodes 4 and 8, respectively, thereby activating the antifuse element.

As noted previously, programming pulses which comprise high electrical voltages may damage various components of an EEPROM, including without limitation the gate oxide layer, transistors and other structures on the surface of the EEPROM. Consequently, in order to reduce the potential for damaging EEPROMs during the programming thereof, the programming pulses for EEPROMs are ever-decreasing, as are the normal operating voltages thereof. State of the art EEPROMs typically operate at either 5V or 3.3V. United States Patent 5,486,707, issued to Kevin T. Look et al. on January 23, 1996, discloses an exemplary programmable memory that includes antifuse elements that may be switched to an "on" state by a programming voltage of about 7.5V to about 10V. While in the "off" state, the electrical resistance of a typical EEPROM antifuse element is on the order of about 1 gigaohm or greater. After an antifuse of a typical state of the art EEPROM has been switched to the "on" state by a programming pulse, the former has a low electrical resistance, on the order of tens of ohms or less.

The memory elements of such state of the art EEPROMs typically have lower programming voltage requirements than their predecessors, due to the structure of the memory elements of the former and the materials that are utilized in the memory

elements. While the programming voltage requirements of such EEPROMs are ever-decreasing, due to the widespread use of conventional, low thermal impedance metal contacts in connection with the antifuse elements thereof, an extremely high current is typically required in order to generate a sufficient temperature to activate such antifuse elements. Further, due to the high rate at which many conventional metal contacts dissipate heat, such contacts may necessitate the input of even greater amounts of current in order to adequately heat and activate an antifuse element. Moreover, the typical use of conventional, relatively large metal contacts on such EEPROMs is somewhat undesirable from the standpoint that such contacts consume a great deal of surface area or "real estate" on the surface of the semiconductor device. Thus, conventional metal contacts limit the density of active device regions on the semiconductor device.

The dissipation of heat away from the memory cell through the metal contact is especially undesirable when the memory cell includes a phase change component, such as a chalcogenide material layer, such as the EEPROM devices disclosed in United States Patent 5,789,758 (hereinafter "the '758 Patent"), which issued to Alan R. Reinberg on August 4, 1998. As is known in the art, chalcogenide materials and some other phase change materials exhibit different electrical characteristics depending upon their state. For example, chalcogenide materials have a lower electrical conductivity in their amorphous state, or phase, than in their crystalline state. Chalcogenide materials may be changed from an amorphous state to a crystalline state by increasing their temperature. The electrical conductivity of the material may vary incrementally between the amorphous state and the crystalline state.

Some EEPROMs include metal contacts that are offset from the active device regions of the former. Such offset contacts are said to reduce the dissipation of thermal energy from the active device regions. Although the direct dissipation of heat from the active device regions of such EEPROM structures may be reduced, thermal energy is conducted to the offset metal contacts, which dissipate heat at approximately the same rate as conventionally positioned metal contacts.

Thus, an electrical and thermal contact is needed which facilitates the input of reduced current and voltage into a structure that is electrically contacted thereto (i.e., conserves energy) and which has a low rate of thermal dissipation relative to conventional metal contacts. A more compact electrical and/or thermal contact structure is also needed.

SUMMARY OF THE INVENTION

The electrical and thermal contact of the present invention addresses each of the foregoing needs. The electrical and thermal contact of the present invention contacts a structure of a semiconductor device, such as a phase change component of an active device region thereof, as disclosed in the '758 Patent, and in United States Patent 5,789,277 ("the '277 Patent"), which issued to Zahorik et al. on August 4, 1998, the disclosures of both of which are hereby incorporated by reference in their entirety. The electrical and thermal contact of the present invention includes an intermediate conductive layer adjacent the contacted structure, a thermal insulator component, which is also referred to as an insulator component, that is adjacent the intermediate conductive layer, and a contact layer that is adjacent the thermal insulator component and which partially contacts the intermediate conductive layer. Preferably, the contact layer and intermediate conductive layer are in electrical and thermal communication with the contacted structure. The thermal insulator component is preferably sandwiched between the intermediate conductive layer and the contact layer, such that the thermal insulator component is substantially enveloped by the intermediate conductive and contact layers. An exemplary active device region to which the electrical and thermal contact of the present invention may be contacted is a memory cell, or element, of an electrically erasable programmable memory (EEPROM) device.

Fabricating the electrical and thermal contact includes forming a dielectric layer around the lateral peripheral portions of a semiconductor device structure to be contacted, patterning the dielectric layer to expose at least a portion of the semiconductor device structure to be contacted, such as an active device region thereof,

depositing a first thin conductive layer, depositing another dielectric layer adjacent the first thin conductive layer, patterning the dielectric layer to define a thermal insulator component, depositing a second thin conductive layer adjacent the thermal insulator component and in electrical communication with the first thin conductive layer, and patterning the first and second thin conductive layers to define the intermediate conductive layer and the contact layer, respectively. The dielectric layer is fabricated from an electrically and thermally conductive material. Preferably, during patterning of the dielectric layer, the first thin conductive layer is utilized as an etch stop. The processes that may be employed to fabricate the electrical and thermal contact facilitate the fabrication of a relatively small electrical and thermal contact, when compared with conventional metal contacts.

Other advantages of the present invention will become apparent to those of ordinary skill in the relevant art through a consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic representation of an exemplary conventional antifuse element;

FIG. 2 is a cross-section of a contact according to the present invention, depicting the association of the contact with a contacted structure on the surface of a semiconductor device;

FIG. 3 is a cross-section of a variation of the semiconductor device of FIG. 2, the contacted structure of which includes a phase change component;

FIG. 4 is a cross-section of a semiconductor device, depicting the formation of a first thin layer of electrically conductive material over the phase change component of FIG. 3;

FIG. 5 is a cross-section of a semiconductor device, depicting the formation of a dielectric layer over the first thin layer of FIG. 4;

FIG. 6 is a cross-section of a semiconductor device, depicting the patterning of the dielectric layer of FIG. 5;

FIG. 7 is a cross-section of a semiconductor device, depicting the formation of a second thin layer of electrically conductive material over the patterned dielectric layer and first thin layer of FIG. 6;

FIG. 8 is a cross-section of a semiconductor device, depicting the patterning of the first and second layers of FIG. 7;

FIG. 9 is a schematic cross-sectional representation of a semiconductor device including a contact according to the present invention which is in contact with a memory element; and

FIG. 10 and 11 are schematic cross-sectional representations of alternative embodiments of the electrical and thermal contact of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention comprises an electrical and thermal contact for a contacted structure of a semiconductor device. With reference to FIGs. 2 and 3, in a preferred embodiment, the electrical and thermal contact 10 is disposed on an surface 15 of a semiconductor device 14. Electrical and thermal contact 10 may be positioned adjacent a contacted structure 12, such as an anti-fuse or other memory element, that is exposed through oxide layer 11, such that it electrically and thermally contacts the contacted structure. Preferably, contact 10 contacts an electrically conductive phase change component 13 of contacted structure 12 (FIG. 3), such as the memory element disclosed in the '578 Patent. Preferably, contacted structure 12 includes a dielectric element 19 surrounding the lateral peripheral portions of phase change component 13 to thermally and electrically insulate the latter.

Electrical and thermal contact 10 includes a thin, intermediate conductive layer 16, disposed adjacent contact structure 12, a thermal insulator component 20 positioned adjacent the intermediate conductive layer, and a thin, electrically conductive contact layer 22 disposed adjacent the thermal insulator component. Preferably,

thermal insulator component 20 is sandwiched between intermediate conductive layer 16 and contact layer 22, such that thermal insulator component 20 is substantially enveloped by the base and contact layers.

Phase change component 13 is preferably fabricated from an electrically conductive phase change material, such as amorphous silicon or a so-called "chalcogenide" alloy, which typically includes at least one of germanium, antimony, selenium, and telurium. Such materials exhibit different electrical characteristics depending upon their state. For example, phase change materials such as chalcogenides exhibit greater electrical conductivity when in a crystalline phase than in an amorphous phase.

Intermediate conductive layer 16 is positioned such that it electrically contacts phase change component 13 and establishes electrical communication between contact layer 22 and contacted structure 12. Intermediate conductive layer 16 is fabricated from an electrically conductive material and preferably has a thickness of about 200Å or less. Preferably, in order to maintain the structural integrity of intermediate conductive layer 16 during the operation of semiconductor device 14, the material from which the intermediate conductive layer is fabricated has a melting point that is higher than both the ambient temperature at which the semiconductor device operates and the phase change temperature of phase change component 13. An exemplary material that may be used to fabricate intermediate conductive layer 16 is titanium nitride (TiN), which may be deposited in highly conformal layers of about 200Å or less by techniques that are known in the art, such as chemical vapor deposition processes. Other materials that may be used to define intermediate conductive layer 16 include, without limitation, tungsten, titanium, other refractory metals, other refractory metal nitrides, metal alloys and other materials which are useful as electrically conductive traces on semiconductor devices.

Thermal insulator component 20 is disposed upon intermediate conductive layer 16, and is preferably positioned over contacted structure 12. Thermal insulator component 20 may be fabricated from a thermally insulative material, such as a silicon

oxide (e.g., SiO_2), a doped silicon oxide (e.g., borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG)), silicon nitride, thermoset resins, thermoplastic polymers, and other dielectric materials which exhibit good thermal insulative properties.

Contact layer 22 is preferably disposed over the entire surface of thermal insulator component 20 and over the exposed portions of intermediate conductive layer 16 that are adjacent to the thermal insulator component. Contact layer 22 is fabricated from an electrically conductive material that preferably has a thickness of about 200Å or less. Preferably, in order to maintain the structural integrity of contact layer 22 during the operation of semiconductor device 14, the material from which the contact layer 22 is fabricated has a melting point that is higher than both the ambient temperature at which the semiconductor device operates and the phase change temperature of phase change component 13. An exemplary material from which contact layer 22 may be fabricated is titanium nitride (TiN), which may be deposited in highly conformal layers of about 200Å or less by techniques that are known in the art, such as chemical vapor deposition processes. Alternatively, contact layer 22 may be manufactured from materials including, without limitation, aluminum, tungsten, titanium, other refractory metals, other refractory metal nitrides, metal alloys and other materials that are useful as electrically conductive traces in semiconductor device applications.

Turning now to FIGs. 4 through 8, a process for fabricating electrical and thermal contact 10 is described and illustrated.

Referring now to FIG. 4, in order to form intermediate conductive layer 16 (*see* FIGs. 2 and 3), a first thin layer 24 of thermally and electrically conductive material is deposited on surface 15 of semiconductor device 14, such that it contacts portions of phase change component 13, that are exposed through the oxide layer of surface 15. First thin layer 24 may be formed by techniques that are known in the art which are capable of depositing an electrically conductive layer formed of a desired material and having a desirable thickness and conformity. Thin-film deposition techniques that are

useful for forming first thin layer 24 include, without limitation, chemical vapor deposition (CVD) processes (e.g., atomospheric pressure CVD, low pressure CVD, plasma-enhanced CVD) and sputtering, or physical vapor deposition, processes. Such techniques typically blanket-deposit a layer of the desired material over the entire surface of a semiconductor device or larger substrate including a multitude of such devices, including any exposed contacted structures thereof.

FIG. 5 illustrates the deposition of a dielectric layer 26 adjacent first thin layer 24. Preferably, dielectric layer 26 is deposited upon first thin layer 24. As described in greater detail below, thermal insulator component 20 (*see* FIGs. 2 and 3) will be defined from dielectric layer 26. Dielectric layer 26, which comprises a thermally insulative material, such as those disclosed previously in reference to FIGs. 2 and 3, may be deposited adjacent first thin layer 24 across the contact by techniques that are known to those in the art, such as chemical vapor deposition processes. Dielectric layer 26 has a thickness that will provide the desired amount of heat retention proximate phase change component 13 at a desirable temperature to effect the desired phase change and consequent change in the electrical conductivity of phase change component 13.

With reference to FIG. 6, dielectric layer 26, which is depicted by broken lines, is patterned to define one or more distinct thermal insulator components 20 of desired dimensions which are positioned in desired locations upon semiconductor device 14. Processes that are known in the art, such as masking and etching, are employed to pattern dielectric layer 26 and define one or more thermal insulator components 20 therefrom. Preferably, first thin layer 24 is utilized as an etch stop while defining one or more thermal insulator components 20 from dielectric layer 26.

Turning to FIG. 7, a second thin layer 28 of thermally and electrically conductive material is then deposited adjacent thermal insulator component 20. Second thin layer 28 is preferably deposited conformally and in substantially uniform thickness over surface 15 of semiconductor device 14 (or larger substrate as noted above), including substantially over the exposed areas of each of the thermal insulator

component 20 and upon the exposed portions of first thin layer 24. Second thin layer 28 may be formed by techniques that are known in the art which are capable of depositing an electrically conductive layer formed of a desired material and having a desirable thickness and conformity. Thin-film deposition techniques that are useful for forming second thin layer 28 include, without limitation, chemical vapor deposition (CVD) processes and sputtering processes. Such techniques typically blanket-deposit a layer of the desired material over the entire surface 15 of semiconductor device 14.

Referring now to FIG. 8, first and second thin layers 24 and 28 are patterned to define intermediate conductive layer 16 and contact layer 22 of each distinct electrical and thermal contact 10 on surface 15, as well as any electrical traces (not shown) that are in electrical contact with the electrical and thermal contacts. First and second thin layers 24 and 28 may be patterned by techniques that are known in the art, such as masking and etching.

The processes that may be employed to fabricate electrical and thermal contact 10 facilitate the fabrication of a structure that is relatively small when compared to the size of conventional metal contacts. Similarly, electrical and thermal contact 10 may be fabricated by processes that form and define structures of various dimensions. The thermal and electrical conductivity of electrical and thermal contact 10 is dependent upon several factors, including, without limitation, the thickness of the first and second thin layers, the height and mass of the thermal insulator, and various characteristics of the materials from which intermediate conductive layer 16, contact layer 22 and thermal insulator component 20 are fabricated.

Referring again to FIG. 3, as noted previously, the disposition of electrical and thermal contact 10 adjacent and in direct contact with phase change component 13 of contacted structure 12 facilitates a reduction in the overall amount of current and heat that are required to operate or activate the contacted structure relative to the respective amount of current that is typically required by many semiconductor devices which include conventional heavy electrical contacts over contacted chalcogenide memory elements. Many conventional electrical contacts dissipate substantial amounts of

thermal energy into the surrounding environment, and thus away from the structures in contact therewith.

In contrast, the thin electrically conductive layers (i.e., intermediate conductive layer 16 and contact layer 22) and the thermal insulator component 20 of electrical and thermal contact 10 effectively retain thermal energy in contacted structure 12. The thin intermediate conductive layer 16 and contact layer 22 each exhibit high impedances relative to conventional metal contacts.

As current is conveyed through contact layer 22 and intermediate conductive layer 16, thermal energy is created and absorbed by phase change component 13. The long path lengths of layers 16 and 22 provide a high thermal impedence and prevent the heat generated in phase change component 13 from being conducted away from phase change component 13. Thus, phase change component 13 heats to a desirable temperature (e.g., a temperature that will switch phase change component 13 from a first conductivity state to a second conductivity state) with a low voltage input relative to that required by conventional metal contacts.

When phase change component 13 is heated to a sufficient temperature, thermal insulator component 20, which is proximate to phase change component 13, opposite intermediate conductive layer 16, prevents heat from escaping into the environment surrounding thermal contact 10 and, therefore, prevents heat from escaping phase change component 13.

Thus, electrical and thermal contact 10 effectively contains thermal energy within phase change component 13 of contacted structure 12. Moreover, due to its small surface area relative to that of conventional metal contacts, electrical and thermal contact 10 does not dissipate heat as quickly as conventional metal contacts. Thus, the amount of voltage that is required to effect a thermally-induced switching of contacted structure 12 from a first state to a second state is also reduced.

FIG. 9 illustrates an exemplary use of electrical and thermal contact 10 in a electrically erasable programmable memory semiconductor device 30, which is also referred to as a semiconductor device for simplicity, that includes a plurality of memory

elements 32 (although only a single memory element 32 is illustrated in FIG. 9). Exemplary memory elements 32 with which the electrical and thermal contact 10 of the present invention are particularly useful include those disclosed in the '758 Patent. Memory element 32 includes an upper contact electrode 36 and a lower contact electrode 38, both of which may comprise a phase change material. As illustrated, memory element 32 also includes diffusion regions of p-doped isolation channels 39 adjacent lower contact electrode 38, and an n-epitaxial structure 40 adjacent the p-doped isolation channel 39. An n+ channel 41, which addresses the individual memory cells 32, is adjacent and in electrical communication with n-epitaxial structure 40. Electrical and thermal contact 10 preferably contacts electrode 36, which may comprise phase change component 13. Although FIG. 9 illustrates a vertically contacted memory element 32, the electrical and thermal contact 10 of the present invention may also be employed in association with other memory element designs or configurations, as are known to those of skill in the art, as well as with other types of memory devices and other structures that may be fabricated on semiconductor devices and for which an infusion of thermal energy with a reduced, or lower, level of current input may be desired.

With continued reference to FIG. 9, as an example of the use of electrical and thermal contact 10 in programming memory element 32, a programming impulse source 42 is placed into electrical contact with contact layer 22. An electrical current generated by source 42 is then conducted through contact layer 22 and intermediate conductive layer 16, and through the phase change component 13 thereof, and causes phase change component 13 to change phase, thereby altering the electrical conductivity characteristics of phase change component 13. Thermal insulator component 20 and low thermal conduction of electrode 36 prevents the escape of heat from memory element 32. Thus, self-heating of the phase change material of phase change component 13, due in part to the resistivity thereof, heats memory element 32 to a temperature that is sufficient to activate the memory element and create a low resistance

electrical pathway through memory element 32, thereby switching memory element 32 from an "off" state to an "on" state.

FIGs. 10 and 11 illustrate alternative embodiments of an electrical and thermal contact 110, 110', respectively, which is disposed on a surface 115, 115', of a semiconductor device 114, 114' in electrical contact with a contacted structure, such as a memory element 112, 112' of a type known in the art.

Electrical and thermal contact 110, 110' includes a thin, electrically conductive base layer 116, 116' disposed on surface 115, 115', of semiconductor device 114, 114' and in electrical contact with a first conductive element 130, 130' of fuse 112, 112'. An insulator component 120, 120' of contact 110, 110' is disposed on base layer 116, 116'. An electrically conductive contact layer 122, 122' is disposed adjacent insulator component 120, 120', and in electrical contact with base layer 116, 116'. Each of the elements of contact 110, 110' may be fabricated from the materials and by the processes that were discussed above.

Memory element 112, 112' includes a memory cell 132, 132' in electrical contact with first conductive element 130, 130'. Fuse element 132, 132' is fabricated as known in the art, from materials such as polysilicon that will undergo a phase change, "rupture," or "fuse" to create a higher or lower electrical resistance pathway upon the application of a minimum predetermined current thereto. Memory element 112' may also include a second electrically conductive element 134' that electrically contacts memory cell 132' (*see* FIG. 11).

As an example of the use of electrical and thermal contact 110, 110' in programming a memory element 112, 112', a programming impulse source 142 is placed into contact with contact layer 122, 122'. An electrical current that is generated by source 142, 142' is then conducted through contact layer 122, 122', to memory element 112, 112'. Heat generated in memory element 112, 112' causes it to switch states. The heat is prevented from leaving the memory element 112, 112' by the low thermal conductivity of structure 110, 110'.

Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. The scope of this invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions and modifications to the invention as disclosed herein which fall within the meaning and scope of the claims are to be embraced thereby.

What is claimed is:

1. A contact for a semiconductor device, comprising:

an intermediate conductive layer in electrical contact with a structure of the semiconductor device;

an insulator component disposed adjacent said intermediate conductive layer; and

an electrically conductive contact layer adjacent said insulator component.

2. The contact of claim 1, wherein said insulator component is sandwiched between said intermediate conductive layer and said contact layer.

3. The contact of claim 1, wherein said intermediate conductive layer and said contact layer substantially envelop said insulator component.

4. The contact of claim 1, wherein said insulator component comprises an insulator material selected from the group comprising undoped silicon dioxide, doped silicon dioxide, silicon nitride, thermoset polymers, and thermoplastic polymers.

5. The contact of claim 1, wherein said intermediate conductive layer comprises an electrically conductive material.

6. The contact of claim 1, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

7. The contact of claim 1, wherein said base layer comprises a material having a melting temperature that is greater than a temperature required to switch a phase change component in electrical communication with the contact between a plurality of states.

8. The contact of claim 1, wherein said intermediate conductive layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

9. The contact of claim 1, wherein said contact layer has a thickness of about 200 angstroms or less.

10. The contact of claim 1, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature required to switch a phase change component in electrical communication with the contact between a plurality of states.

11. The contact of claim 1, wherein said contact layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

12. A contact for a memory element of a semiconductor device that includes a phase change component, the contact comprising:

an insulator component comprising a thermally and electrically insulative material;

an intermediate conductive layer adjacent said insulator component and in electrical and thermal communication with the phase change component; and

a contact layer adjacent said insulator component and in electrical contact with said intermediate conductive layer, said contact layer and said intermediate conductive layer substantially enveloping said insulator component.

13. The contact of claim 12, wherein said thermally and electrically insulative material is selected from the group comprising undoped silicon dioxide, doped silicon dioxide, silicon nitride, thermoset resins, and thermoplastic polymers.

14. The contact of claim 12, wherein said intermediate conductive layer comprises an electrically conductive material.

15. The contact of claim 12, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

16. The contact of claim 12, wherein said intermediate conductive layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of the phase change component from a first state to a second state.

17. The contact of claim 12, wherein said intermediate conductive layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

18. The contact of claim 12, wherein said contact layer has a thickness of about 200 angstroms or less.

19. The contact of claim 12, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of the phase change component from a first state to a second state.

20. The contact of claim 12, wherein said contact layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

21. A process for fabricating a contact on a semiconductor device, comprising:

forming a first layer of conductive material on a surface of the semiconductor device and in electrical and thermal communication with a structure thereof;

depositing a dielectric layer on said first layer;

patterning said dielectric layer to define an insulator component;

forming a second layer of conductive material substantially over an exposed area of said insulator component; and

patterning said first layer and said second layer.

22. The process of claim 21, wherein said forming a first layer comprises forming a material layer having a thickness of about 200 angstroms or less.

23. The process of claim 21, wherein said forming a first layer comprises depositing a conductive material.

24. The process of claim 23, wherein said depositing comprises chemical vapor deposition.

25. The process of claim 23, wherein said depositing comprises physical vapor deposition.

26. The process of claim 21, wherein said patterning said dielectric layer comprises etching and employs said first layer as an etch stop.

27. The process of claim 21, wherein said forming a second layer comprises forming a material layer having a thickness of about 200 angstroms or less.

28. The process of claim 21, wherein said forming a second layer comprises depositing a conductive material.

29. The process of claim 28, wherein said depositing comprises chemical vapor deposition.

30. The process of claim 28, wherein said depositing comprises physical vapor deposition.

31. The process of claim 21, wherein said forming a first layer comprises disposing a conductive material in electrical and thermal communication with a phase change component of said structure.

32. A contact for a semiconductor device including a contact layer and an intermediate conductive layer which partially contact one another and substantially envelop an insulator component, fabricated by the process comprising:

forming the intermediate conductive layer on a surface of the semiconductor device and in electrical thermal communication with an active device region of the semiconductor device;

depositing a dielectric layer on the intermediate conductive layer;

patterning said dielectric layer to define the insulator component;

forming the contact layer substantially over an exposed area of the insulator component and in electrical communication with the intermediate conductive layer;

patterning the intermediate conductive layer; and

patterning the contact layer.

33. The process of claim 32, wherein said forming the intermediate conductive layer comprises disposing a conductive material in electrical and thermal communication with a phase change component of said active device region.

34. The contact of claim 32, wherein said forming the intermediate conductive layer comprises forming a thermally conductive material layer having a thickness of about 200 angstroms or less.

35. The contact of claim 32, wherein said forming the intermediate conductive layer comprises depositing a thermally conductive material.

36. The contact of claim 32, wherein said patterning said dielectric layer comprises etching and employs the intermediate conductive layer as an etch stop.

37. The contact of claim 32, wherein said forming the contact layer comprises forming an electrically conductive material layer having a thickness of about 200 angstroms or less.

38. The process of claim 32, wherein said forming the contact layer comprises depositing an electrically conductive material.

39. An electrically erasable programmable memory device, comprising:

a memory element including an electrode adjacent a memory cell, at least one of said first electrode and said memory cell comprising a phase change material; and

a contact including an intermediate conductive layer in electrical and thermal communication with said phase change material, an insulator component adjacent said intermediate conductive layer, and a contact layer adjacent said insulator component and in electrical communication with said intermediate conductive layer.

40. The programmable read-only memory device of claim 39, wherein said intermediate conductive layer contacts said electrode.

41. The programmable read-only memory device of claim 39, wherein said contact layer and said intermediate conductive layer substantially envelop said insulator component.

42. The programmable read-only memory device of claim 39, wherein said insulator component is sandwiched between said contact layer and said intermediate conductive layer.

43. The programmable read-only memory device of claim 39, wherein said contact layer has a thickness of about 200 angstroms or less.

44. The programmable read-only memory device of claim 39, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

45. A semiconductor device including at least one contact, the contact comprising:

an intermediate conductive layer in electrical and thermal communication with a phase change component of a structure of the semiconductor device;

an insulator component disposed adjacent said intermediate conductive layer; and

a contact layer adjacent said insulator component and in electrical communication with said intermediate conductive layer.

46. The semiconductor device of claim 45, wherein said insulator component is sandwiched between said intermediate conductive layer and said contact layer.

47. The semiconductor device of claim 44, wherein said intermediate conductive layer and said contact layer substantially envelop said insulator component.

48. The semiconductor device of claim 45, wherein said insulator component comprises a thermally insulative material.

49. The semiconductor device of claim 45, wherein said intermediate conductive layer comprises an electrically conductive material.

50. The semiconductor device of claim 45, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

51. The semiconductor device of claim 45, wherein said intermediate conductive layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of states.

52. The semiconductor device of claim 45, wherein said intermediate conductive layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

53. The semiconductor device of claim 45, wherein said contact layer has a thickness of about 200 angstroms or less.

54. The semiconductor device of claim 45, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of states.

55. The semiconductor device of claim 45, wherein said contact layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

56. An enhanced electrically erasable programmable element including a contact comprising:

an intermediate conductible layer in electrical contact with a structure of the semiconductor device;

an insulator component disposed adjacent said intermediate conductive layer; and

an electrically conductive contact layer adjacent said insulator component.

57. The enhanced electrically erasable programmable element of claim 56, wherein said insulator component is sandwiched between said intermediate conductive layer and said contact layer.

58. The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer and said contact layer substantially envelop said insulator component.

59. The enhanced electrically erasable programmable element of claim 56, wherein said insulator component comprises a thermally insulative material.

60. The enhanced electrically erasable programmable element of claim 56, wherein said insulator component comprises thermally insulative material selected from the group comprising undoped silicon dioxide, doped silicon dioxide, silicon nitride, thermoset resins, and thermoplastic polymers.

61. The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer comprises an electrically conductive material.

62. The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer has a thickness of about 200 angstroms or less.

63. The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of electrical conductivity states.

64. The enhanced electrically erasable programmable element of claim 56, wherein said intermediate conductive layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

65. The enhanced electrically erasable programmable element of claim 56, wherein said contact layer has a thickness of about 200 angstroms or less.

66. The enhanced electrically erasable programmable element of claim 56, wherein said contact layer comprises a material having a melting temperature that is greater than a temperature that is required to switch a phase change material of a contacted structure between a plurality of states.

67. The enhanced electrically erasable programmable element of claim 56, wherein said contact layer comprises a material selected from the group comprising refractory metals, refractory metal nitrides, and aluminum.

ABSTRACT

An electrical and thermal contact for use in a semiconductor device. The electrical and thermal contact includes an intermediate conductive layer, an insulator component, and a contact layer. The intermediate conductive layer may contact a structure of the semiconductor device. The insulator component, which is fabricated from a thermally and electrically insulative material, may be sandwiched between the intermediate conductive layer and the contact layer, which may substantially envelop the insulator component. The electrical and thermal contact may be fabricated by a process which includes forming a first thin layer on a surface of the semiconductor device, depositing a dielectric layer adjacent the first thin layer, patterning the dielectric layer to define the insulator component, forming a second thin layer adjacent the insulator component and in partial contact with the first thin layer, and patterning the first and second thin layers to define the intermediate conductive layer and the contact layer, respectively. Due to its structure, which requires relatively little electrical current to generate a desired amount of heat, the electrical and thermal contact effectively contains heat within and prevents heat from dissipating from a contacted structure, and is particularly useful for contacting and inducing a change in the electrical conductivity of structures which include phase change materials.

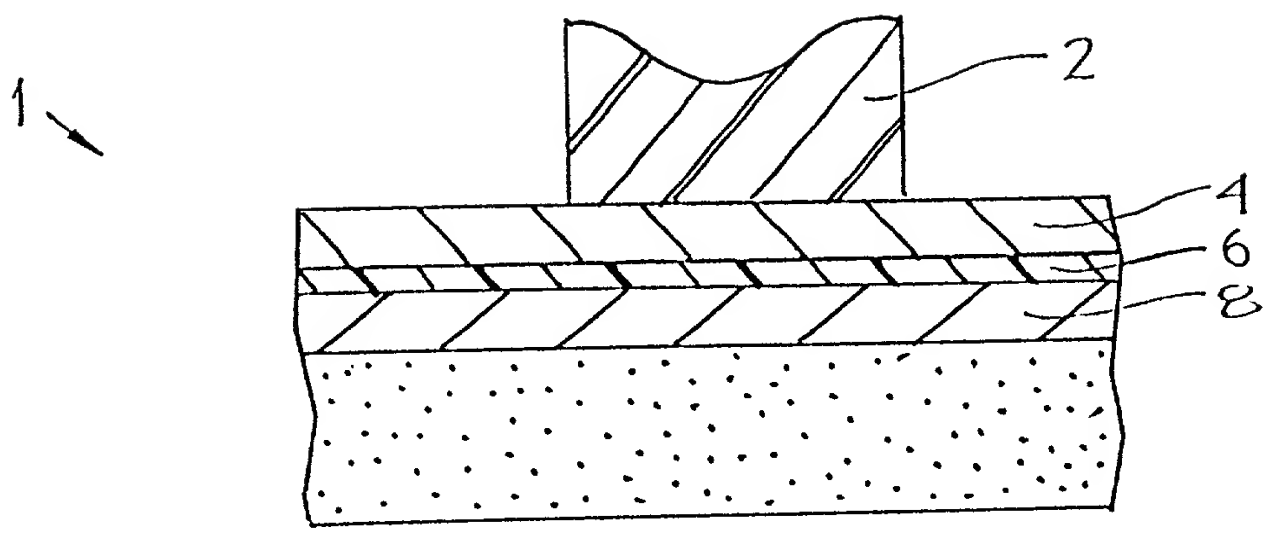


FIG. 1

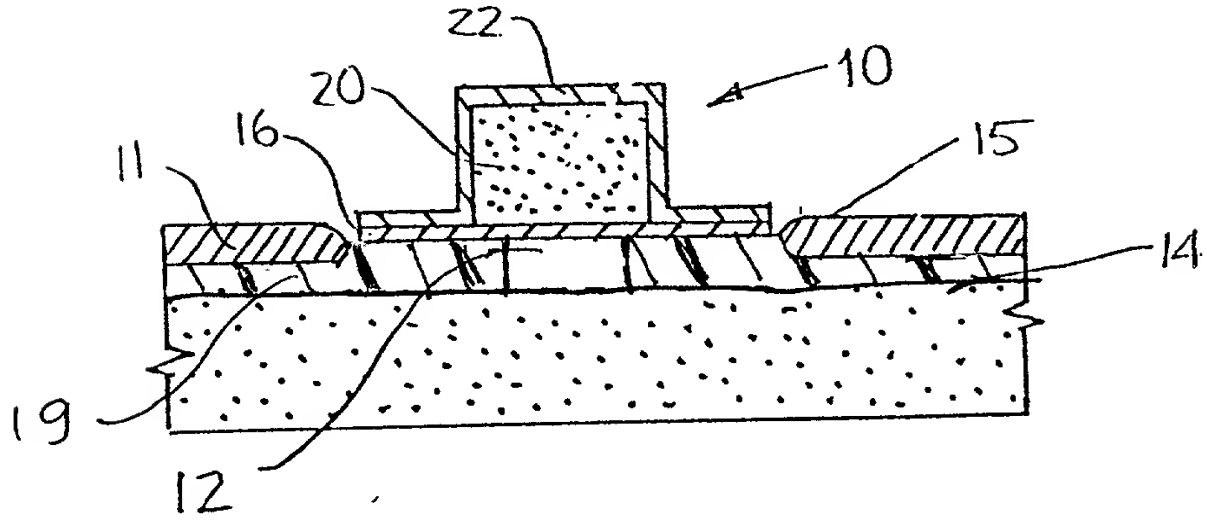


FIG. 2

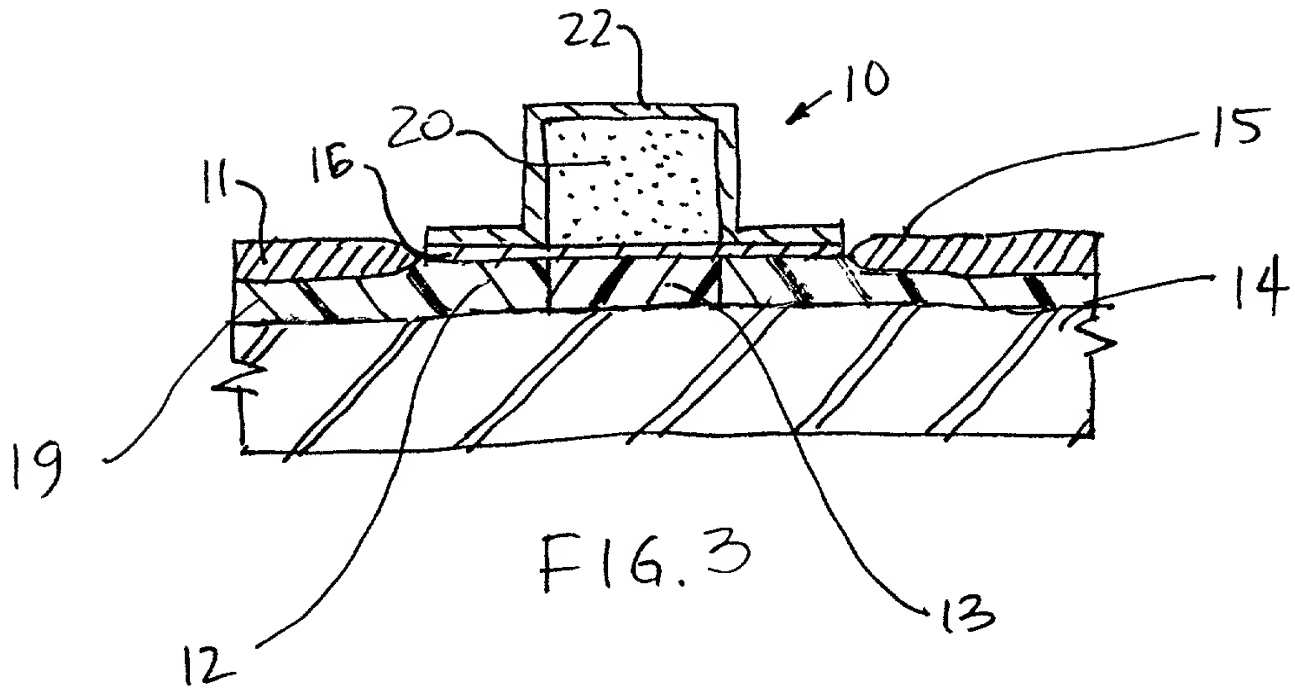


FIG. 3

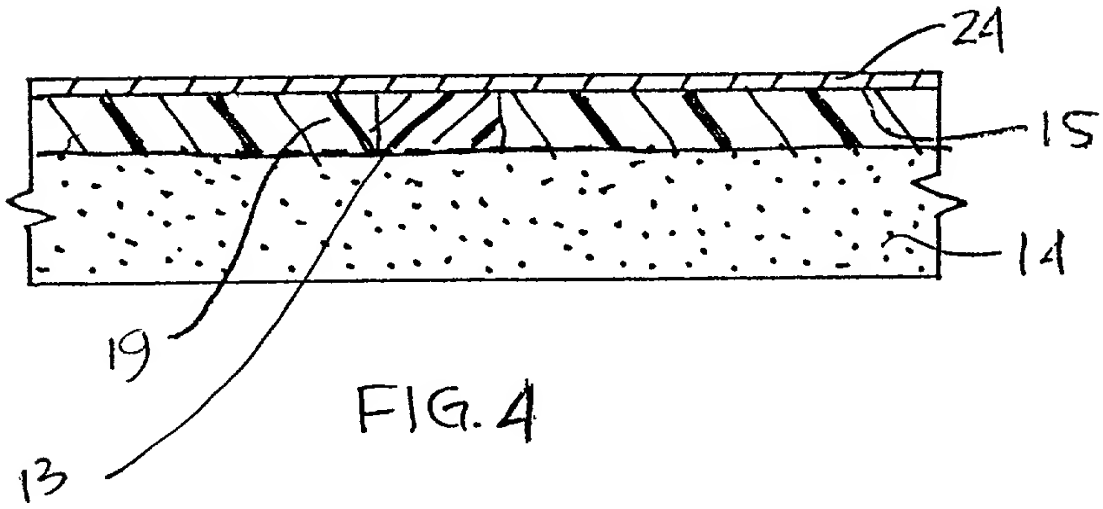


FIG. 4

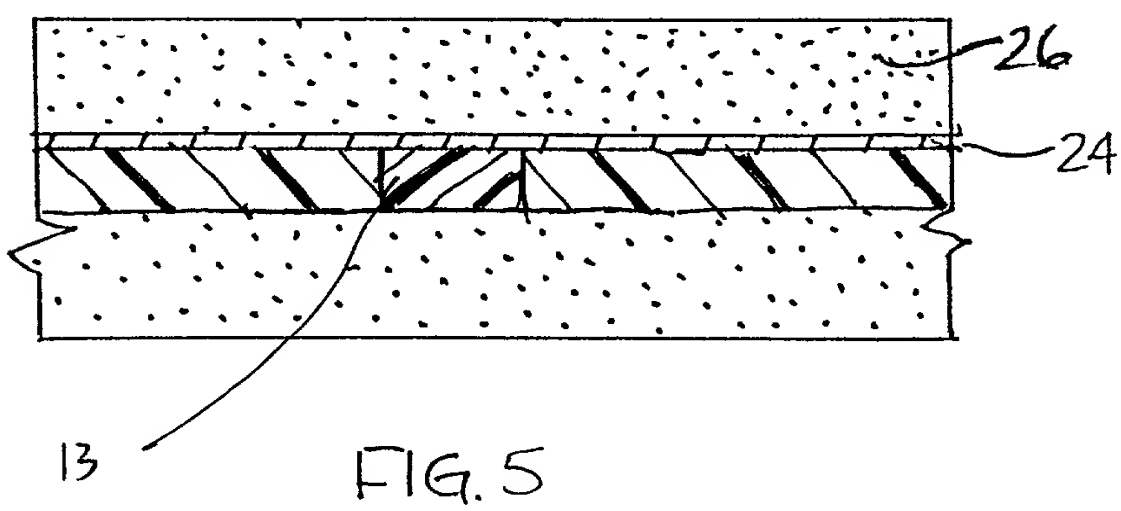


FIG. 5

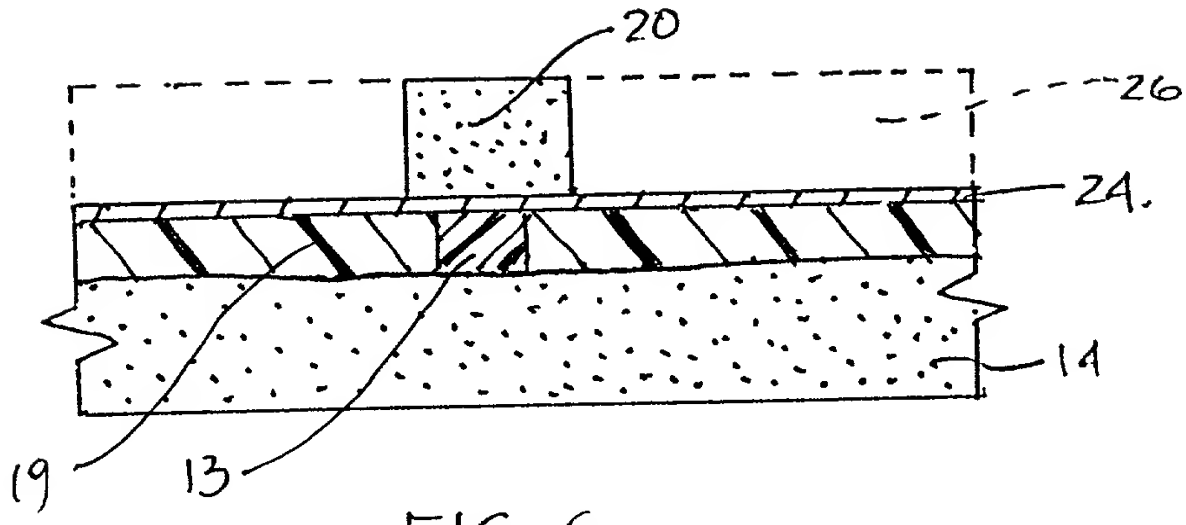


FIG. 6

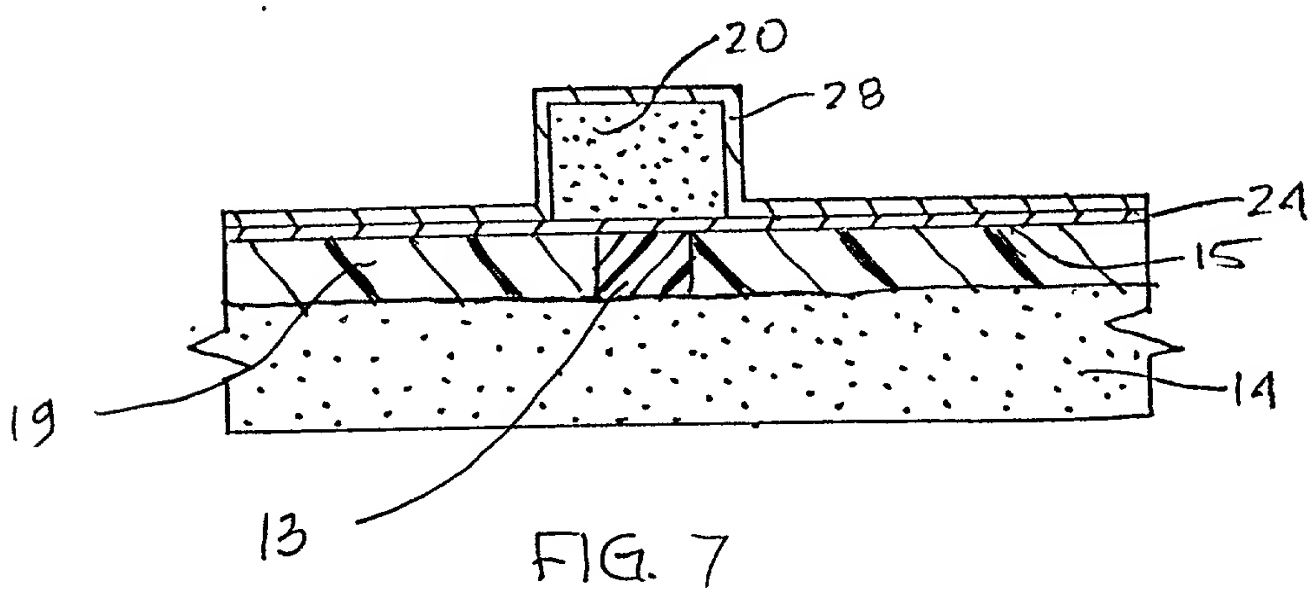


FIG. 7

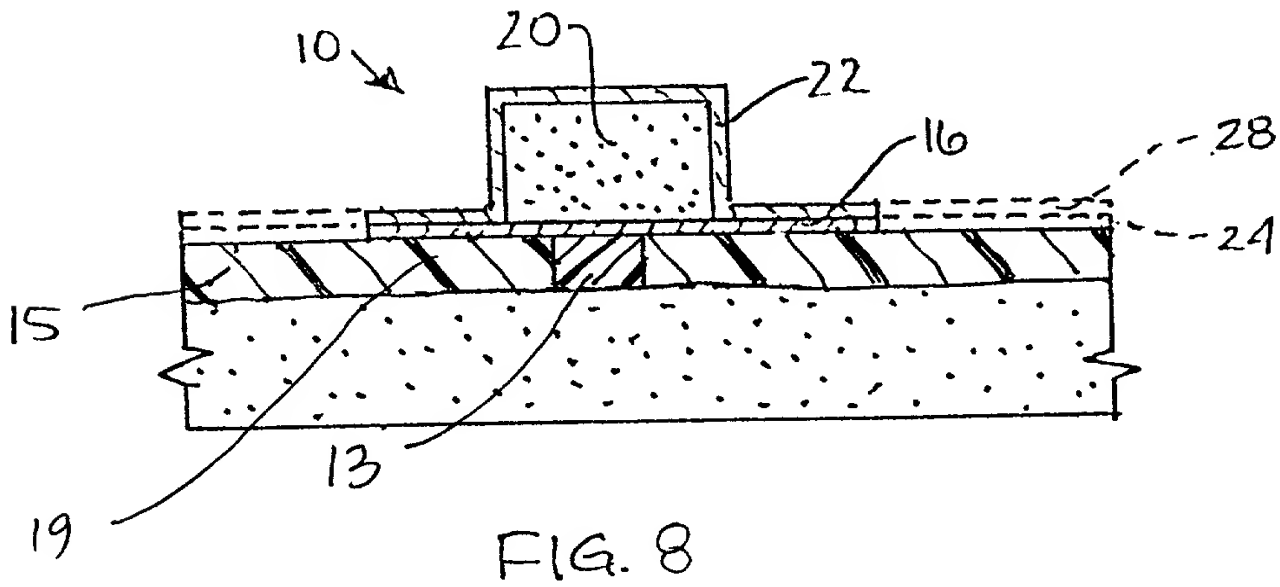


FIG. 8

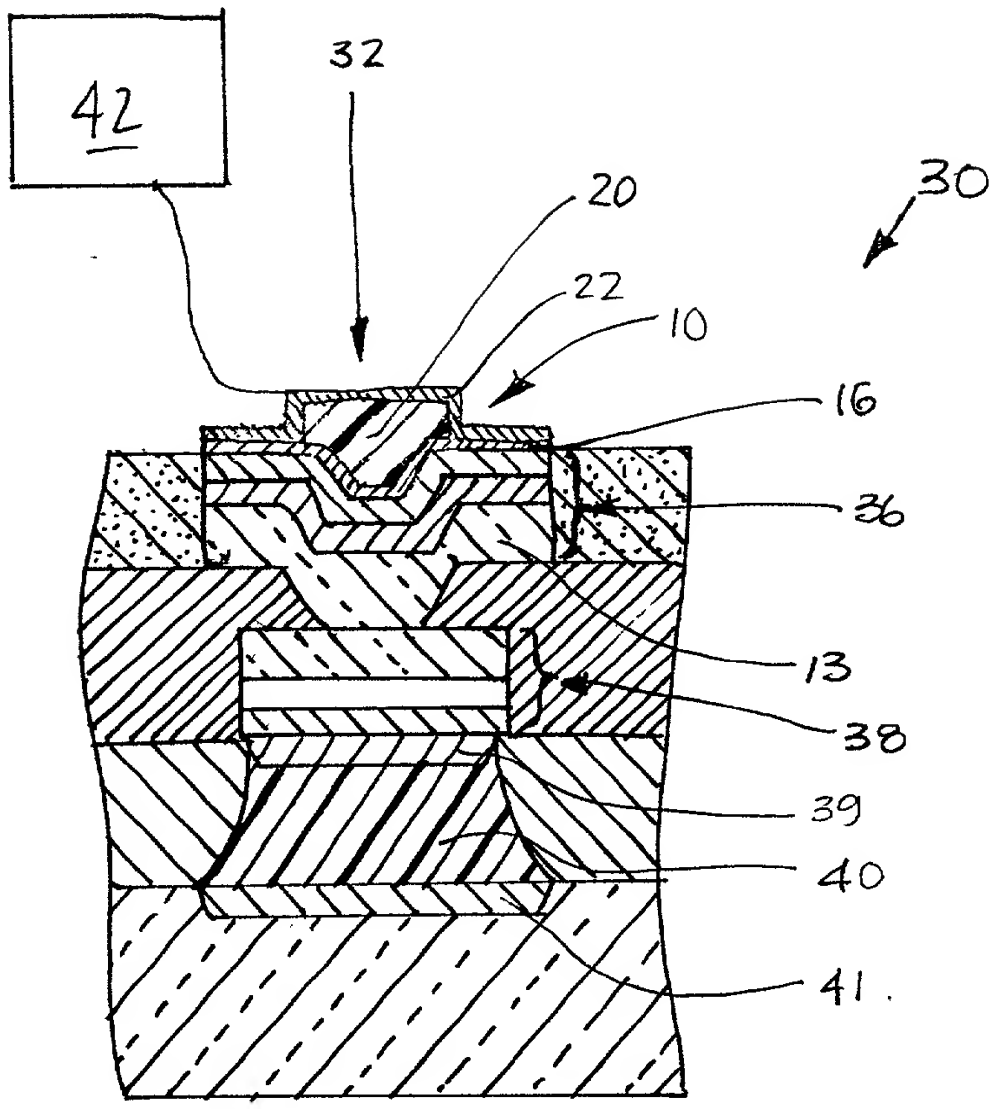
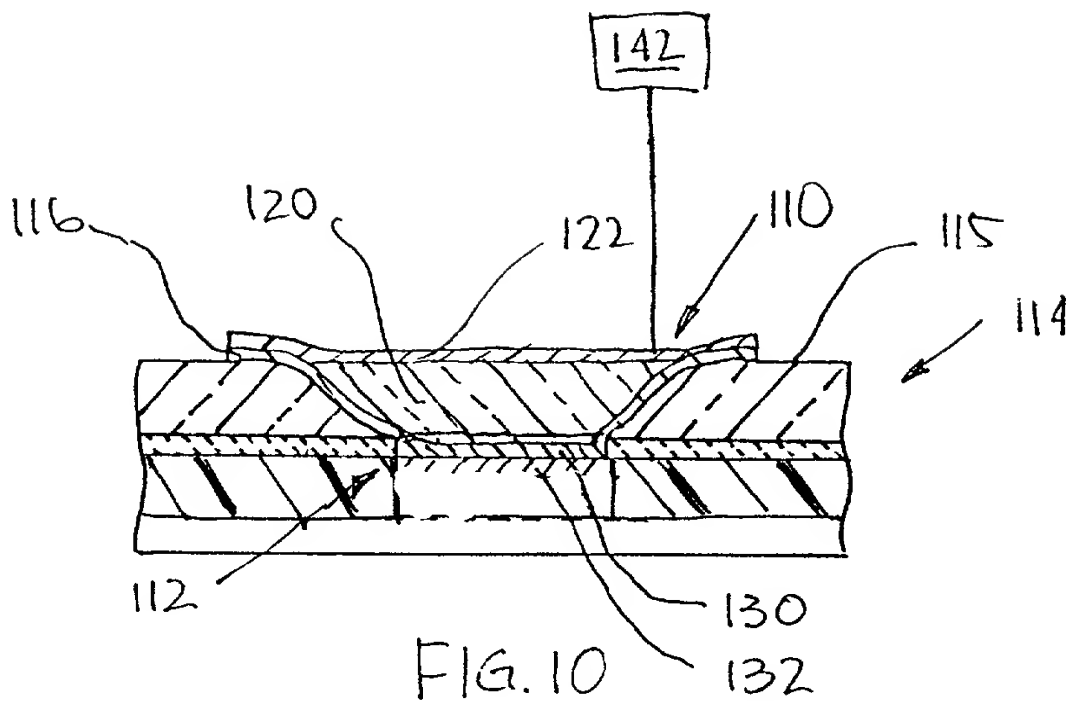


FIG.9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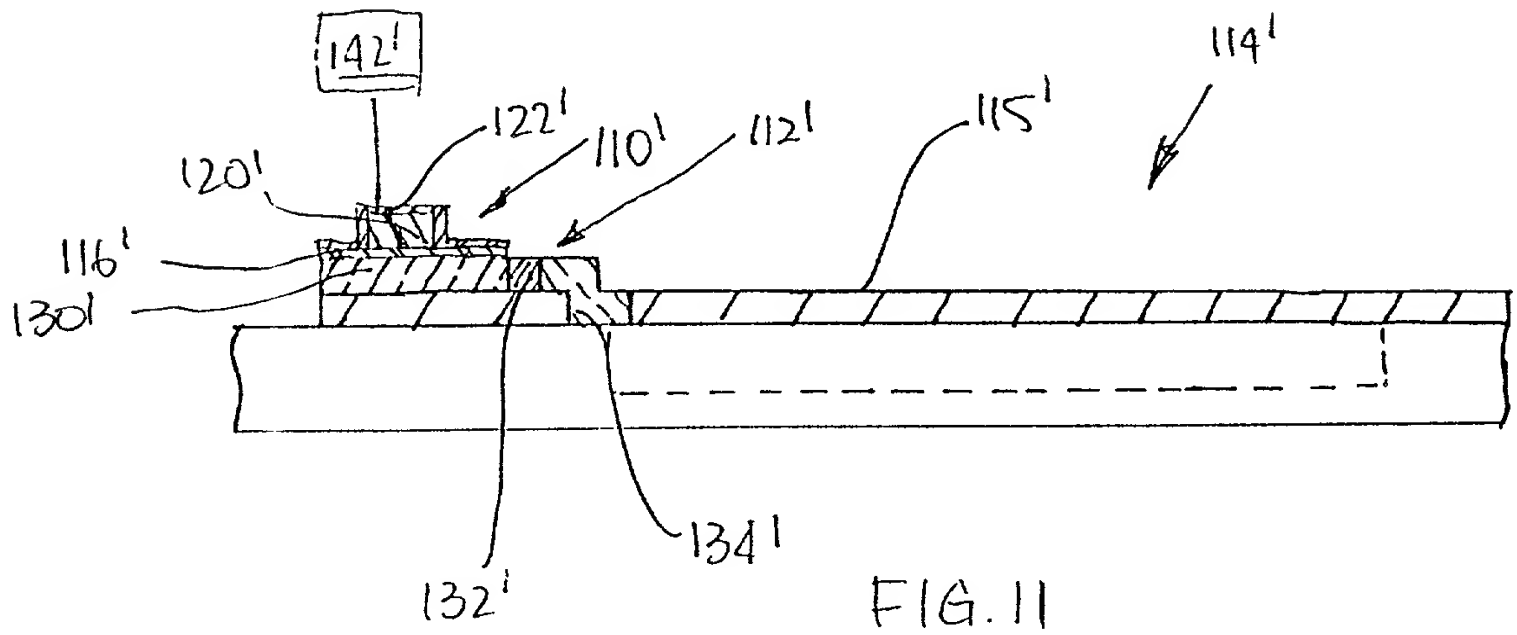
132

FIG. 10


142'
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112'
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114'
120'
116'
130'
132'
134'

FIG. 11

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan R. Reinberg
Serial No.:
Filed:
Title: ELECTRICAL AND THERMAL CONTACT FOR USE IN SEMICONDUCTOR DEVICES

Examiner:
Group Art Unit:
Attorney Docket No.: 3528US (97-1099)

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Julie K. Morriss, Reg. No. 33,263
Robert G. Winkle, Reg. No. 37,474	Patrick McBride, Reg. No. 39,295	Edgar R. Cataxinos, Reg. No. 39,931
Kenneth E Horton, Reg. No. 39,481	Brick G. Power, Reg. No. 38,581	Kenneth Booth, Reg No. 43,342
Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095	

as its attorneys with full power of substitution to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

[] In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .

[x] In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to.

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P.O. Box 2550
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Fax: (801) 531-9168

Respectfully Submitted,

MICRON TECHNOLOGY, INC.

Date. October 15, 1998

By:_____
Michael L. Lynch, Esq.
Reg. No. 30,871
Chief Patent Counsel,
MICRON TECHNOLOGY, INC.

N:\2269\3528\Power of Attorney.wpd

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled ELECTRICAL AND THERMAL CONTACT FOR USE IN SEMICONDUCTOR DEVICES, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
(provisional application no.)	(filing date)
(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012
Laurence B. Bond, Reg. No. 30,549
Allen C. Turner, Reg. No. 33,041
Robert G. Winkle, Reg. No. 37,474
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Patrick McBride, Reg. No. 39,295
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Edgar R. Cataxinos, Reg. No. 39,931
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Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Alan R. Reinberg
Inventor's signature _____ Date Oct 20, 1998
Residence: Westport, Connecticut
Citizenship: U.S.A.
Post Office Address: 6 Terhune Drive, Westport, CT 06880